

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A communications acquisition method, which comprises:

correlating a received binary-coded spread sequence arriving at a frequency f and having m bits with a locally generated spread sequence having m bits, the locally generated spread sequence having k sections, the correlating step comprising the following steps:

storing the received binary-coded spread sequence,

splitting the stored received binary-coded spread sequence into k sections, each of the k sections including more than one bit, and

correlating the k sections of the stored received binary-coded spread sequence at a frequency $k*f$ with corresponding k sections of the locally generated spread sequence, wherein m and k are integers greater than 1, and k is smaller than m .

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Claim 2 (previously presented): The method according to claim 1, which further comprises:

upon correlating each section of the stored received binary-coded spread sequence, shifting the bits of a respective section by one bit to replace the least significant bit of a first section variant by a succeeding bit of the received binary-coded spread sequence and to shift a most significant bit of a the first section variant to a position of the least significant bit of a succeeding section variant.

Claim 3 (canceled):

Claim 4 (previously presented): A correlator for performing a communications acquisition, comprising:

a FIFO memory having a memory input and a memory output, said FIFO memory inputting and outputting a content;

a shift register with feedback for holding a received signal sequence in serial form, said shift register having register positions connected in parallel to said memory input for parallel storage of a plurality of shift register contents read out in succession, said memory output being connected in

parallel with said register positions for parallel transfer of data to said shift register;

a further memory for holding reference signal sequences; and

a comparator for comparing the content of said FIFO memory with a content of said further memory;

the correlator programmed to perform the step of:

correlating a binary-coded spread sequence arriving at a frequency f and having m bits with a locally generated spread sequence by

storing the received binary-coded spread sequence, splitting the stored received binary-coded spread sequence into k sections; and

correlating the sections of the stored received binary-coded spread sequence at a frequency of $k*f$ with corresponding sections of the locally generated spread sequence.

Claim 5 (original): The correlator according to claim 4, wherein said comparator has a comparator output, and including an adder comprising two-bit adders configured to form a cascaded interconnection, each of said two-bit adders having

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at least two inputs and an output, said output of each of said two-bit adders connected to one of said at least two inputs of a succeeding one of said two-bit adders, said adder connected to said comparator output and configured to add up logic values produced during bit-by-bit comparison for matching bit positions.

Claim 6 (previously presented): The method according to claim 2, which further comprises:

summing the correlation results obtained per section correlation step over k section correlation steps to obtain a count result;

repeating the shifting step $m-1$ times for obtaining $m-1$ count results; and

carrying out a maximum search over all the m count results.--

Claim 7 (previously presented): The method according to claim 6, wherein a number of sections of prescribed length is $k=32$ and a chip length of the sections is $n=32$.